PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2000-285071

(43)Date of publication of application : 13.10.2000

(51)Int.Cl. G06F 13/42

G06F 1/04

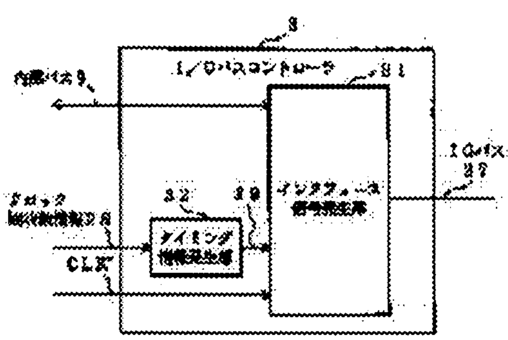
(21)Application number : 11-094328

(22)Date of filing : 31.03.1999

(71)Applicant : TOSHIBA CORP

(72)Inventor : AIZAWA HIDEO

(54) COMPUTER SYSTEM



(57)Abstract:

PROBLEM TO BE SOLVED: To reduce power consumption without reducing the processing speed of an extended device by controlling the change timing of an interface signal.

SOLUTION: A clock supply part sets up reference clock frequency lower than normal frequency and transmits the set clock frequency information 28 to an I/O bus controller 8. A timing information generation part 32 in the controller 8 recognizes current clock frequency from the inputted information 28, calculates timing information 29 for changing an interface signal by converting the information into clock frequency and transmits the information 29 to an interface signal generation part 31. The generation part 31 prepares an interface signal on the basis of the information 29 and accesses an extended device, e.g. KBCont.

LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

* NOTICES *

JPO and INPIT are not responsible for any damages caused by the use of this translation.

1.This document has been translated by computer. So the translation may not reflect the original precisely.

2.**** shows the word which can not be translated.

3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to the computing system which controls the data transmission rate of asynchronous buses, such as an ISA Bus, based on a reference clock.

[0002]

[Description of the Prior Art] From the former, although power-saving is advanced with the miniaturization, when a computing system, for example, a personal computer etc., makes a personal computer a power-saving condition, in order that the processing speed to an extended device may also fall, an improvement is desired.

[0003] The input/output interface control section, for example, an I/O bus controller etc., is prepared in the conventional computer system. In this I/O bus controller, if the frequency of a basic clock is made low, the whole equipment can be changed into a power-saving condition. However, the change timing of an interface signal will become large in this case, and the processing speed to an extended device will fall sharply.

[0004] Here, the reason is explained with reference to drawing 6 and drawing 7 . Drawing showing the data write-in actuation to the extended device at the time of the normal operation of the I/O bus controller of the former [drawing 6] and drawing 7 are drawings showing the data write-in actuation to the extended device at the time of power saving.

[0005] In drawing 6 , CLK is a clock signal. CS# is a selection signal.

[0006] An extended device will recognize being accessed, if this signal is set to L level. WR# is a write strobe signal. If this signal is set to L level, an extended device will recognize that it is write-in actuation, and will input the value of a data signal. DATA is a data signal.

[0007] Moreover, time amount T10 is time amount after CS# falls to L level until WR# falls to L level. Time amount T20 shows the time amount from which WR# has L level. Time amount T30 shows time amount after WR# starts on H level until CS# starts on H level.

[0008] The hour entry which shows the change timing of the interface signal doubled with change of the frequency information on a clock signal is called timing information. Timing information here is T10, T20, and T30, and if it converts into the number of clocks to count, it will be set to (2), (4), and (1), respectively.

[0009] Thus, in the conventional I/O bus controller which operates, if the frequency of a basic clock is set to usual 1/2 in order to reduce power consumption, since the power for

making a basic clock will end few, power consumption can be reduced as the whole computing system. however, the part from which the clock frequency fell also in the timing of each data processing since the timing information T11, T21, and T31 converted into the number of clocks was also the set point (2) as it is, (4), and (1) as shown in drawing 7 -- it becomes late and the processing speed to an extended device falls sharply.

[0010]

[Problem(s) to be Solved by the Invention] This invention is for solving such a technical problem, and it aims at offering the computing system which can reduce power consumption, without reducing the processing speed to an extended device.

[0011]

[Means for Solving the Problem] In order to attain the purpose mentioned above, the computing system of invention according to claim 1 In the computing system which controls data transfer to the extended device connected to the I/O bus based on the clock signal used as criteria, while supplying the frequency to each part in a system free [adjustable], said clock signal A clock supply means to output the frequency information on said clock signal, and a timing information generating means to change the timing information for counting said clock signal according to the frequency information outputted from said clock supply means, It is characterized by providing a means to count the clock signal supplied from said clock supply means based on the timing information which changed with said timing information generating means, and to generate the interface signal to said I/O bus.

[0012] In the computer system which controls data transfer to the extended device connected to the I/O bus based on the clock signal with which the computer system of invention according to claim 2 serves as criteria While issuing the directions to which a clock signal is changed to a clock supply means to supply the frequency for said clock signal to each part in a system free [adjustable], and said clock supply means The control means which outputs the frequency information on said clock signal, and a timing information generating means to change the timing information for counting said clock signal according to the frequency information outputted from said control means, It is characterized by providing a means to count the clock signal supplied from said clock supply means based on the timing information which changed with said timing information generating means, and to generate the interface signal to said I/O bus.

[0013] In the computing system according to claim 2, as for the computing system of invention according to claim 3, said timing information generating means is characterized by providing a frequency information maintenance means to hold the frequency information outputted from said control means, and the timing information generating section which generates the timing information for counting said clock signal according to the frequency information held by said frequency information maintenance means.

[0014] In the computer system which controls data transfer to the extended device connected to the I/O bus based on the clock signal with which the computer system of invention according to claim 4 serves as criteria While issuing the directions to which a clock signal is changed to a clock supply means to supply the frequency for said clock signal to each part in a system free [adjustable], and said clock supply means The control means which outputs the timing information for counting said clock signal according to the frequency information on said clock signal, It is characterized by providing a means to count the clock signal supplied from said clock supply means based

on the timing information outputted from said control means, and to generate the interface signal to said I/O bus.
[0015] According to change of the frequency information on a basic clock, adjustable [of the change timing of an interface signal] is carried out, and the data transfer rate of asynchronous buses, such as an ISA Bus connected to the extended device, for example, a keyboard controller, is controlled by this invention.
[0016] That is, it can change to a power-saving condition from a normal operating state, and the frequency of a basic clock can reduce power consumption, without reducing the data transfer rate to an extended device, since it also makes counted value of a basic clock small in the form doubled with it when change, for example, a frequency, is made low.
[0017]
[Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is explained to a detail with reference to a drawing. Drawing showing outline configurations, such as the computing system of the 1st operation gestalt which drawing 1 requires for this invention, for example, a personal computer etc., (a personal computer is called below), and drawing 2 are drawings showing the important section configuration of this computing system.
[0018] This computer system is a bus controller 1, the display controller 2, a graphics accelerator 3, the USB host controller 4, the VRAM controller 5, the PCMCIA controller 6, and Smart. The Media controller 7, the I/O bus controller 8, As the register interface bus 9, the VRAM interface bus 10, the clock controller 11, the interruption controller 12, a system memory 20, and a control means It has the ** processor 21, the power control circuit 22, ROM23 and VRAM24, the keyboard controller 25 (KBCont.25 are called below), etc.
[0019] A bus controller 1, the display controller 2, a graphics accelerator 3, the USB host controller 4, the VRAM controller 5, the PCMCIA controller 6, Smart As a device controller 100, inside one IC chip, each module mounting is carried out and the Media controller 7, the I/O bus interface controller 8 (the I/O bus controller 8 is called below), the register interface bus 9, the VRAM interface bus 10, the clock controller 11, the interruption controller 12, etc. are formed into 1 chip.
[0020] A bus controller 1 changes a system bus into an internal bus. The display controller 2 performs control for displaying on the LCD panel or CRT. A graphics accelerator 3 improves a display speed. The USB host controller 4 controls the connected USB device. The VRAM controller 5 controls VRAM24. The PCMCIA controller 6 controls the connected card device. The SmartMedia controller 7 controls the connected flash memory. The I/O bus controller 8 performs control of KBCont.25 and the extended device connected in addition to this. The register interface bus 9 is an internal bus used for internal register access etc. That is, the register interface bus 9 is used for the data transmission between the registers of each module connected inside the device controller 100. The VRAM interface bus 10 is a bus which connects the device which accesses VRAM24. The clock controller 11 performs control of the clock source or the clock gate. For example, the clock signal CLK supplied from the clock feed zone 26 is supplied to each module in a device controller 100. Moreover, the supplied clock signal CLK is changed into clock signal CLK' for I/O bus controller 8, and it transmits to the I/O bus controller 8. The interruption controller 12 performs discernment and control of

effective/invalid for an interruption factor. The interruption controller 12 controls the interrupt signal from a keyboard etc. The DRAM system memory 20 memorizes the various programs and constant datas of procedure including a program concerning employment of this equipment. Based on the program stored in the DRAM system memory 20, a processor 21 performs overall control of this equipment, and performs data processing to various kinds of data inputted from a keyboard etc. The power control circuit 22 controls system-wide supply voltage. MROM23 stores the application program for raising the use effectiveness of an interface. VRAM24 memorizes the various data displayed on a display device by the bitmapped image. KBCont.25 are one of the extended devices, code the key information inputted from the keyboard, and transmit it to the I/O bus controller 8. The clock feed zone 26 controls the frequency of a clock signal by the instruction of a processor 21. Moreover, while inputting a clock signal CLK into the clock controller 11, the frequency information 28 on a clock signal CLK (clock frequency information) is inputted to the I/O bus controller 8. I/O bus 27 is a bus which transmits an interface signal between the I/O-bus interface controller 8 and KBCont.25 which are an extended device.

[0021] As shown in drawing 2 , the I/O bus controller 8 has the interface signal generator 31 and the timing information generating section 32. The interface signal generator 31 changes into an interface signal the directions of a processor 21 received through the register interface bus 9, and is accessed with KBCont.25 through I/O bus 27. The timing information generating section 32 computes the timing information to which an interface signal is changed based on the frequency information on the clock signal inputted from the clock feed zone 26, and transmits it to the interface signal generator 31. In addition, how to carry out the multiplication of the scale factor of the clock frequency at that time to the timing value at the time of the usual clock frequency as the calculation approach of timing information, and revalue for an integer can be considered. However, as long as it is the timing to be able to KBCont.operate, other approaches [approach / of timing information / calculation] may be used.

[0022] Next, with reference to drawing 3 , actuation of the computing system of this 1st operation gestalt is explained.

[0023] If system-wide throughput becomes less, in order to cut down power consumption, a processor 21 will control the clock feed zone 26 to make a clock frequency lower than the usual frequency.

[0024] The clock feed zone 26 is controlled by the processor 21, and the clock frequency information 28 which shows that a current clock frequency is usual 1/2 is transmitted to the I/O bus controller 8 at the same time it is lower than the usual frequency in a frequency, for example, it sets to 1/2 etc. the basic clock CLK used as the criteria on which a device controller 100 operates and it supplies the clock controller 11. This clock frequency information 28 is inputted into the timing information generating section 32 in the I/O bus controller 8.

[0025] If the clock frequency information 28 is inputted into the timing information generating section 32, the timing information 29 over the frequency of clock CLK' into which the timing information generating section 32 has recognized that a current clock frequency is usual 1/2, and it was inputted from the clock frequency information 28 will be computed. For example, the timing information generating section 32 computes the set point for counting clock CLK' with the value, 1, 2, and 1, of the usual one half, and tells

this timing information 29 to the interface signal generator 31 in the I/O bus controller 8. [i.e.,] The interface signal generator 31 makes an interface signal based on the inputted timing information 29, and accesses KBCont.25 through I/O bus 27.

[0026] Drawing 3 is drawing showing the interface signal when lowering a clock frequency to usual 1/2.

[0027] In this drawing, CLK' is a clock signal inputted from the clock controller 11. CS# is a selection signal.

[0028] KBCont.25 which are an extended device will recognize being accessed, if this selection-signal CS# is set to L level. WR# is a write strobe signal. If this write strobe signal WR# is set to L level, KBCont.25 will recognize that it is write-in actuation, and will input the value of a data signal. DATA is a data signal.

[0029] Moreover, T12 is time amount after selection-signal CS# falls to L level until write strobe signal WR# falls to L level. T22 shows the time amount from which write strobe signal WR# has L level. T32 shows time amount after write strobe signal WR# starts on H level until selection-signal CS# starts on H level.

[0030] The hour entry which shows the change timing of the interface signal doubled with change of clock signal CLK', i.e., change of the clock frequency information 28, is timing information 29. Here, this timing information 29 is T12, T22, and T32, and if it converts into the number of clocks to count, it will be set to (1), (2), and (1), respectively.

[0031] When it is [at the time] low to about 1/2 and the frequency of the basic clock CLK of the whole system is usually carried out, as it is shown in drawing 3 , as for clock signal CLK' inputted into the I/O bus controller 8, the period Tck doubles (Tckx2).

[0032] With this operation gestalt, in the I/O bus controller 8, the value of the timing information 29 for counting clock signal CLK' to compensate for change of clock signal CLK' and the change timing of the interface signal outputted from the I/O bus controller 8 since it is made small will become small, and the processing speed to KBCont.25 will not be different from before power saving.

[0033] Thus, according to the computer system of this 1st operation gestalt, adjustable [of the value of the timing information 29 for counting clock signal CLK' to compensate for change of clock signal CLK' from the clock controller 11] is carried out to the I/O bus controller 8 by having formed the timing information generating section 32. For example, when it is 1/2 of the usual clock frequency, the change timing of the interface signal outputted from the I/O bus controller 8 will also become small, and the processing speed to KBCont.25 will not change it to 1/2 to before power saving.

[0034] Thereby, power consumption can be reduced, without reducing the processing speed to KBCont.25 (extended device).

[0035] Next, the computing system of the 2nd operation gestalt which starts this invention with reference to drawing 4 is explained. Drawing 4 is drawing showing the I/O bus controller 48 of the computer system of the 2nd operation gestalt of this invention.

[0036] As shown in this drawing, this I/O bus controller 48 has the interface signal generator 31, the timing information generating section 32, and a register 33.

[0037] In this case, the clock frequency information 28 is inputted into the interface signal generator 31 and a register 33 through an internal bus 9 from a processor 21. Therefore, the timing information generating section 32 will read the clock frequency information 28 set as the register 33 in this case.

[0038] In the case of the computer system of this 2nd operation gestalt, the clock frequency information 28 is set as the register 33 in the I/O bus controller 48 through an internal bus 9 from a processor 21. The timing information generating section 32 reads the clock frequency information 28 set as the register 33, generates timing information 29, and outputs it to the interface signal generator 31.
[0039] Thus, since it is not necessary to output the clock frequency information 28 from the clock feed zone 26 while the same effectiveness as the above-mentioned 1st operation gestalt is acquired, since according to the computer system of this 2nd operation gestalt the clock frequency information 28 from a processor 21 is set as a register 33, the timing information generating section 32 reads the clock frequency information 28 on this register 33 and timing information 29 is generated, this invention is realizable after considering the clock feed zone 26 as a comparatively simple configuration.
[0040] Next, the computing system of the 3rd operation gestalt which starts this invention with reference to drawing 5 is explained. Drawing 5 is drawing showing the I/O bus controller 58 of the computer system of the 3rd operation gestalt of this invention.
[0041] This 3rd operation gestalt is the example which built in the timing information register 34 instead of the timing information generating section 32 of the above-mentioned 1st and 2nd operation gestalt.
[0042] As shown in this drawing, this I/O bus controller 58 consists of only an interface signal generator 31 and a timing information register 34.
[0043] This example is an example using the calculation function by the side of a processor 21. That is, since processor 21 self usually directs modification of a clock frequency to the clock feed zone 26 when making the whole equipment into a power-saving condition, the processor 21 knows the value of the clock frequency information to change. Then, the interface signal generator 31 reads each timing information 28 which the processor 21 computed each timing information 28 based on the value of clock frequency information in this case, held this computed timing information 28 to the timing information register 34 of the I/O bus controller 58 through the internal bus 9, and was held at this timing information register 34, and an interface signal is generated.
[0044] By doing in this way, according to the computer system of this 3rd operation gestalt, while the same effectiveness as the above-mentioned 1st operation gestalt is acquired, the configuration of the I/O bus controller 58 can be simplified.
[0045] In addition, it is not limited only to each above-mentioned operation gestalt.
[0046] Although the above-mentioned operation gestalt showed the example which formed the clock feed zone 26 in the exterior of a device controller 100, the clock feed zone 26 may be arranged that is, built in the interior of the I/O bus controller 8.
[0047] Moreover, memory, such as FP-DRAM and SRAM, is connected to the I/O bus controller 8, and the same effectiveness can be acquired even if it makes it operate the I/O bus controller 8 as a memory controller.
[0048] Furthermore, by giving the function to stop the clock to the applicable section to it, while the I/O bus controller 8 is not operating for the clock controller 11, when a clock is lowered, the number of clocks needed while the I/O bus controller 8 operates can be reduced (when it is made to change).
[0049] Thereby, system-wide power consumption can be reduced.
[0050]
[Effect of the Invention] As it ****(ed) above, according to this invention, according to

change of the frequency information on a basic clock, adjustable [of the change timing of an interface signal] is carried out, and the data transfer rate of the extended device connected to the I/O bus is controlled.

[0051] The frequency of a basic clock can sometimes reduce power consumption by following, for example, changing the whole system from a normal operating state to a power-saving condition, without reducing the data transfer rate to an extended device, since it also makes counted value of a basic clock small in the form doubled with it when change, for example, a frequency, is made low.

[Translation done.]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

CLAIMS

[Claim(s)]
[Claim 1] In the computing system which controls data transfer to the extended device connected to the I/O bus based on the clock signal used as criteria, while supplying the frequency to each part in a system free [adjustable], said clock signal A clock supply means to output the frequency information on said clock signal, and a timing information generating means to change the timing information for counting said clock signal according to the frequency information outputted from said clock supply means, The computing system characterized by providing a means to count the clock signal supplied from said clock supply means based on the timing information which changed with said timing information generating means, and to generate the interface signal to said I/O bus.
[Claim 2] In the computing system which controls data transfer to the extended device connected to the I/O bus based on the clock signal used as criteria While issuing the directions to which a clock signal is changed to a clock supply means to supply the frequency for said clock signal to each part in a system free [adjustable], and said clock supply means The control means which outputs the frequency information on said clock signal, and a timing information generating means to change the timing information for counting said clock signal according to the frequency information outputted from said control means, The computing system characterized by providing a means to count the clock signal supplied from said clock supply means based on the timing information which changed with said timing information generating means, and to generate the interface signal to said I/O bus.
[Claim 3] It is the computing system characterized by providing the timing information generating section which generates the timing information for counting said clock signal according to the frequency information held by frequency information maintenance means to hold the frequency information to which said timing information generating means was outputted from said control means in the computing system according to claim 2, and said frequency information maintenance means.

[Claim 4] In the computing system which controls data transfer to the extended device connected to the I/O bus based on the clock signal used as criteria While issuing the directions to which a clock signal is changed to a clock supply means to supply the frequency for said clock signal to each part in a system free [adjustable], and said clock supply means The control means which outputs the timing information for counting said clock signal according to the frequency information on said clock signal, The computing system characterized by providing a means to count the clock signal supplied from said clock supply means based on the timing information outputted from said control means, and to generate the interface signal to said I/O bus.

[Translation done.]

TECHNICAL FIELD

[Field of the Invention] This invention relates to the computing system which controls the data transmission rate of asynchronous buses, such as an ISA Bus, based on a reference clock.

[Translation done.]

PRIOR ART

[Description of the Prior Art] From the former, although power-saving is advanced with the miniaturization, when a computing system, for example, a personal computer etc., makes a personal computer a power-saving condition, in order that the processing speed to an extended device may also fall, an improvement is desired.
[0003] The input/output interface control section, for example, an I/O bus controller etc., is prepared in the conventional computer system. In this I/O bus controller, if the frequency of a basic clock is made low, the whole equipment can be changed into a power-saving condition. However, the change timing of an interface signal will become large in this case, and the processing speed to an extended device will fall sharply.
[0004] Here, the reason is explained with reference to drawing 6 and drawing 7 . Drawing showing the data write-in actuation to the extended device at the time of the normal operation of the I/O bus controller of the former [drawing 6] and drawing 7 are drawings showing the data write-in actuation to the extended device at the time of power saving.
[0005] In drawing 6 , CLK is a clock signal. CS# is a selection signal.
[0006] An extended device will recognize being accessed, if this signal is set to L level. WR# is a write strobe signal. If this signal is set to L level, an extended device will recognize that it is write-in actuation, and will input the value of a data signal. DATA is a data signal.

[0007] Moreover, time amount T10 is time amount after CS# falls to L level until WR# falls to L level. Time amount T20 shows the time amount from which WR# has L level. Time amount T30 shows time amount after WR# starts on H level until CS# starts on H level.
[0008] The hour entry which shows the change timing of the interface signal doubled with change of the frequency information on a clock signal is called timing information. Timing information here is T10, T20, and T30, and if it converts into the number of clocks to count, it will be set to (2), (4), and (1), respectively.
[0009] Thus, in the conventional I/O bus controller which operates, if the frequency of a basic clock is set to usual 1/2 in order to reduce power consumption, since the power for making a basic clock will end few, power consumption can be reduced as the whole computing system. however, the part from which the clock frequency fell also in the timing of each data processing since the timing information T11, T21, and T31 converted into the number of clocks was also the set point (2) as it is, (4), and (1) as shown in drawing 7 -- it becomes late and the processing speed to an extended device falls sharply.

[Translation done.]

EFFECT OF THE INVENTION

[Effect of the Invention] As it ****(ed) above, according to this invention, according to change of the frequency information on a basic clock, adjustable [of the change timing of an interface signal] is carried out, and the data transfer rate of the extended device connected to the I/O bus is controlled.
[0051] The frequency of a basic clock can sometimes reduce power consumption by following, for example, changing the whole system from a normal operating state to a power-saving condition, without reducing the data transfer rate to an extended device, since it also makes counted value of a basic clock small in the form doubled with it when change, for example, a frequency, is made low.

[Translation done.]

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] This invention is for solving such a technical problem, and it aims at offering the computing system which can reduce power consumption, without reducing the processing speed to an extended device.

[Translation done.]

MEANS

[Means for Solving the Problem] In order to attain the purpose mentioned above, the computing system of invention according to claim 1 In the computing system which controls data transfer to the extended device connected to the I/O bus based on the clock signal used as criteria, while supplying the frequency to each part in a system free [adjustable], said clock signal A clock supply means to output the frequency information on said clock signal, and a timing information generating means to change the timing information for counting said clock signal according to the frequency information outputted from said clock supply means, It is characterized by providing a means to count the clock signal supplied from said clock supply means based on the timing information which changed with said timing information generating means, and to generate the interface signal to said I/O bus.
[0012] In the computer system which controls data transfer to the extended device connected to the I/O bus based on the clock signal with which the computer system of invention according to claim 2 serves as criteria While issuing the directions to which a clock signal is changed to a clock supply means to supply the frequency for said clock signal to each part in a system free [adjustable], and said clock supply means The control means which outputs the frequency information on said clock signal, and a timing information generating means to change the timing information for counting said clock signal according to the frequency information outputted from said control means, It is characterized by providing a means to count the clock signal supplied from said clock supply means based on the timing information which changed with said timing information generating means, and to generate the interface signal to said I/O bus.
[0013] In the computing system according to claim 2, as for the computing system of invention according to claim 3, said timing information generating means is characterized by providing a frequency information maintenance means to hold the frequency information outputted from said control means, and the timing information generating section which generates the timing information for counting said clock signal according to the frequency information held by said frequency information maintenance means.
[0014] In the computer system which controls data transfer to the extended device connected to the I/O bus based on the clock signal with which the computer system of invention according to claim 4 serves as criteria While issuing the directions to which a clock signal is changed to a clock supply means to supply the frequency for said clock signal to each part in a system free [adjustable], and said clock supply means The control means which outputs the timing information for counting said clock signal according to the frequency information on said clock signal, It is characterized by providing a means to count the clock signal supplied from said clock supply means based on the timing information outputted from said control means, and to generate the interface signal to said I/O bus.
[0015] According to change of the frequency information on a basic clock, adjustable [of the change timing of an interface signal] is carried out, and the data transfer rate of

asynchronous buses, such as an ISA Bus connected to the extended device, for example, a keyboard controller, is controlled by this invention.

[0016] That is, it can change to a power-saving condition from a normal operating state, and the frequency of a basic clock can reduce power consumption, without reducing the data transfer rate to an extended device, since it also makes counted value of a basic clock small in the form doubled with it when change, for example, a frequency, is made low.

[0017]

[Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is explained to a detail with reference to a drawing. Drawing showing outline configurations, such as the computing system of the 1st operation gestalt which drawing 1 requires for this invention, for example, a personal computer etc., (a personal computer is called below), and drawing 2 are drawings showing the important section configuration of this computing system.

[0018] This computer system is a bus controller 1, the display controller 2, a graphics accelerator 3, the USB host controller 4, the VRAM controller 5, the PCMCIA controller 6, and Smart. The Media controller 7, the I/O bus controller 8, As the register interface bus 9, the VRAM interface bus 10, the clock controller 11, the interruption controller 12, a system memory 20, and a control means It has the ** processor 21, the power control circuit 22, ROM23 and VRAM24, the keyboard controller 25 (KBCont.25 are called below), etc.

[0019] A bus controller 1, the display controller 2, a graphics accelerator 3, the USB host controller 4, the VRAM controller 5, the PCMCIA controller 6, Smart As a device controller 100, inside one IC chip, each module mounting is carried out and the Media controller 7, the I/O bus interface controller 8 (the I/O bus controller 8 is called below), the register interface bus 9, the VRAM interface bus 10, the clock controller 11, the interruption controller 12, etc. are formed into 1 chip.

[0020] A bus controller 1 changes a system bus into an internal bus. The display controller 2 performs control for displaying on the LCD panel or CRT. A graphics accelerator 3 improves a display speed. The USB host controller 4 controls the connected USB device. The VRAM controller 5 controls VRAM24. The PCMCIA controller 6 controls the connected card device. The SmartMedia controller 7 controls the connected flash memory. The I/O bus controller 8 performs control of KBCont.25 and the extended device connected in addition to this. The register interface bus 9 is an internal bus used for internal register access etc. That is, the register interface bus 9 is used for the data transmission between the registers of each module connected inside the device controller 100. The VRAM interface bus 10 is a bus which connects the device which accesses VRAM24. The clock controller 11 performs control of the clock source or the clock gate. For example, the clock signal CLK supplied from the clock feed zone 26 is supplied to each module in a device controller 100. Moreover, the supplied clock signal CLK is changed into clock signal CLK' for I/O bus controller 8, and it transmits to the I/O bus controller 8. The interruption controller 12 performs discernment and control of effective/invalid for an interruption factor. The interruption controller 12 controls the interrupt signal from a keyboard etc. The DRAM system memory 20 memorizes the various programs and constant datas of procedure including a program concerning employment of this equipment. Based on the program stored in the DRAM system

memory 20, a processor 21 performs overall control of this equipment, and performs data processing to various kinds of data inputted from a keyboard etc. The power control circuit 22 controls system-wide supply voltage. MROM23 stores the application program for raising the use effectiveness of an interface. VRAM24 memorizes the various data displayed on a display device by the bitmapped image. KBCont.25 are one of the extended devices, code the key information inputted from the keyboard, and transmit it to the I/O bus controller 8. The clock feed zone 26 controls the frequency of a clock signal by the instruction of a processor 21. Moreover, while inputting a clock signal CLK into the clock controller 11, the frequency information 28 on a clock signal CLK (clock frequency information) is inputted to the I/O bus controller 8. I/O bus 27 is a bus which transmits an interface signal between the I/O-bus interface controller 8 and KBCont.25 which are an extended device.

[0021] As shown in drawing 2 , the I/O bus controller 8 has the interface signal generator 31 and the timing information generating section 32. The interface signal generator 31 changes into an interface signal the directions of a processor 21 received through the register interface bus 9, and is accessed with KBCont.25 through I/O bus 27. The timing information generating section 32 computes the timing information to which an interface signal is changed based on the frequency information on the clock signal inputted from the clock feed zone 26, and transmits it to the interface signal generator 31. In addition, how to carry out the multiplication of the scale factor of the clock frequency at that time to the timing value at the time of the usual clock frequency as the calculation approach of timing information, and revalue for an integer can be considered. However, as long as it is the timing to be able to KBCont.operate, other approaches [approach / of timing information / calculation] may be used.

[0022] Next, with reference to drawing 3 , actuation of the computing system of this 1st operation gestalt is explained.

[0023] If system-wide throughput becomes less, in order to cut down power consumption, a processor 21 will control the clock feed zone 26 to make a clock frequency lower than the usual frequency.

[0024] The clock feed zone 26 is controlled by the processor 21, and the clock frequency information 28 which shows that a current clock frequency is usual 1/2 is transmitted to the I/O bus controller 8 at the same time it is lower than the usual frequency in a frequency, for example, it sets to 1/2 etc. the basic clock CLK used as the criteria on which a device controller 100 operates and it supplies the clock controller 11. This clock frequency information 28 is inputted into the timing information generating section 32 in the I/O bus controller 8.

[0025] If the clock frequency information 28 is inputted into the timing information generating section 32, the timing information 29 over the frequency of clock CLK' into which the timing information generating section 32 has recognized that a current clock frequency is usual 1/2, and it was inputted from the clock frequency information 28 will be computed. For example, the timing information generating section 32 computes the set point for counting clock CLK' with the value, 1, 2, and 1, of the usual one half, and tells this timing information 29 to the interface signal generator 31 in the I/O bus controller 8. [i.e.,] The interface signal generator 31 makes an interface signal based on the inputted timing information 29, and accesses KBCont.25 through I/O bus 27.

[0026] Drawing 3 is drawing showing the interface signal when lowering a clock

frequency to usual 1/2.
[0027] In this drawing, CLK' is a clock signal inputted from the clock controller 11. CS# is a selection signal.
[0028] KBCont.25 which are an extended device will recognize being accessed, if this selection-signal CS# is set to L level. WR# is a write strobe signal. If this write strobe signal WR# is set to L level, KBCont.25 will recognize that it is write-in actuation, and will input the value of a data signal. DATA is a data signal.
[0029] Moreover, T12 is time amount after selection-signal CS# falls to L level until write strobe signal WR# falls to L level. T22 shows the time amount from which write strobe signal WR# has L level. T32 shows time amount after write strobe signal WR# starts on H level until selection-signal CS# starts on H level.
[0030] The hour entry which shows the change timing of the interface signal doubled with change of clock signal CLK', i.e., change of the clock frequency information 28, is timing information 29. Here, this timing information 29 is T12, T22, and T32, and if it converts into the number of clocks to count, it will be set to (1), (2), and (1), respectively.
[0031] When it is [at the time] low to about 1/2 and the frequency of the basic clock CLK of the whole system is usually carried out, as it is shown in drawing 3 , as for clock signal CLK' inputted into the I/O bus controller 8, the period Tck doubles (Tckx2).
[0032] With this operation gestalt, in the I/O bus controller 8, the value of the timing information 29 for counting clock signal CLK' to compensate for change of clock signal CLK' and the change timing of the interface signal outputted from the I/O bus controller 8 since it is made small will become small, and the processing speed to KBCont.25 will not be different from before power saving.
[0033] Thus, according to the computer system of this 1st operation gestalt, adjustable [of the value of the timing information 29 for counting clock signal CLK' to compensate for change of clock signal CLK' from the clock controller 11] is carried out to the I/O bus controller 8 by having formed the timing information generating section 32. For example, when it is 1/2 of the usual clock frequency, the change timing of the interface signal outputted from the I/O bus controller 8 will also become small, and the processing speed to KBCont.25 will not change it to 1/2 to before power saving.
[0034] Thereby, power consumption can be reduced, without reducing the processing speed to KBCont.25 (extended device).
[0035] Next, the computing system of the 2nd operation gestalt which starts this invention with reference to drawing 4 is explained. Drawing 4 is drawing showing the I/O bus controller 48 of the computer system of the 2nd operation gestalt of this invention.
[0036] As shown in this drawing, this I/O bus controller 48 has the interface signal generator 31, the timing information generating section 32, and a register 33.
[0037] In this case, the clock frequency information 28 is inputted into the interface signal generator 31 and a register 33 through an internal bus 9 from a processor 21. Therefore, the timing information generating section 32 will read the clock frequency information 28 set as the register 33 in this case.
[0038] In the case of the computer system of this 2nd operation gestalt, the clock frequency information 28 is set as the register 33 in the I/O bus controller 48 through an internal bus 9 from a processor 21. The timing information generating section 32 reads the clock frequency information 28 set as the register 33, generates timing information

29, and outputs it to the interface signal generator 31.
[0039] Thus, since it is not necessary to output the clock frequency information 28 from the clock feed zone 26 while the same effectiveness as the above-mentioned 1st operation gestalt is acquired, since according to the computer system of this 2nd operation gestalt the clock frequency information 28 from a processor 21 is set as a register 33, the timing information generating section 32 reads the clock frequency information 28 on this register 33 and timing information 29 is generated, this invention is realizable after considering the clock feed zone 26 as a comparatively simple configuration.
[0040] Next, the computing system of the 3rd operation gestalt which starts this invention with reference to drawing 5 is explained. Drawing 5 is drawing showing the I/O bus controller 58 of the computer system of the 3rd operation gestalt of this invention.
[0041] This 3rd operation gestalt is the example which built in the timing information register 34 instead of the timing information generating section 32 of the above-mentioned 1st and 2nd operation gestalt.
[0042] As shown in this drawing, this I/O bus controller 58 consists of only an interface signal generator 31 and a timing information register 34.
[0043] This example is an example using the calculation function by the side of a processor 21. That is, since processor 21 self usually directs modification of a clock frequency to the clock feed zone 26 when making the whole equipment into a power-saving condition, the processor 21 knows the value of the clock frequency information to change. Then, the interface signal generator 31 reads each timing information 28 which the processor 21 computed each timing information 28 based on the value of clock frequency information in this case, held this computed timing information 28 to the timing information register 34 of the I/O bus controller 58 through the internal bus 9, and was held at this timing information register 34, and an interface signal is generated.
[0044] By doing in this way, according to the computer system of this 3rd operation gestalt, while the same effectiveness as the above-mentioned 1st operation gestalt is acquired, the configuration of the I/O bus controller 58 can be simplified.
[0045] In addition, it is not limited only to each above-mentioned operation gestalt.
[0046] Although the above-mentioned operation gestalt showed the example which formed the clock feed zone 26 in the exterior of a device controller 100, the clock feed zone 26 may be arranged that is, built in the interior of the I/O bus controller 8.
[0047] Moreover, memory, such as FP-DRAM and SRAM, is connected to the I/O bus controller 8, and the same effectiveness can be acquired even if it makes it operate the I/O bus controller 8 as a memory controller.
[0048] Furthermore, by giving the function to stop the clock to the applicable section to it, while the I/O bus controller 8 is not operating for the clock controller 11, when a clock is lowered, the number of clocks needed while the I/O bus controller 8 operates can be reduced (when it is made to change).
[0049] Thereby, system-wide power consumption can be reduced.

[Translation done.]

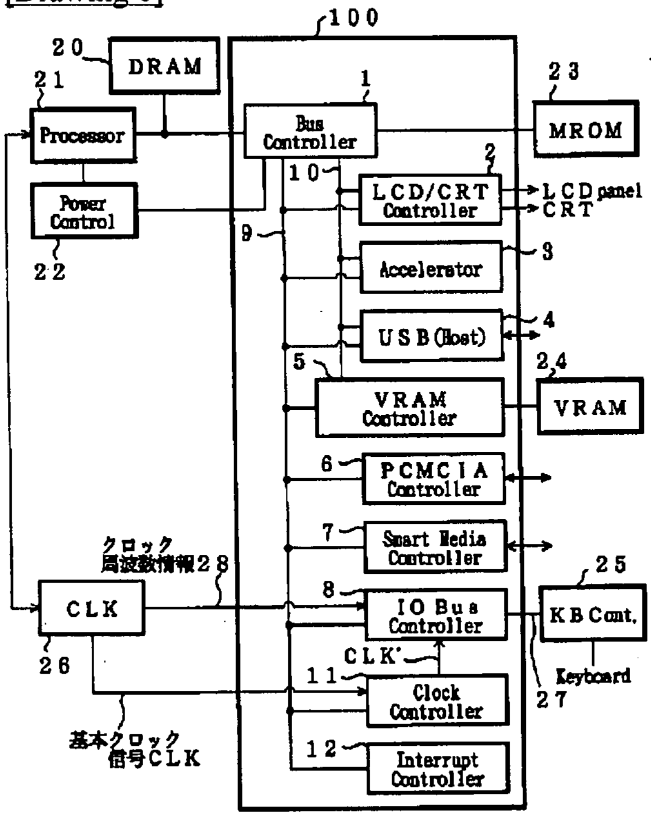
DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] Drawing showing the whole computing system configuration concerning this invention.
[Drawing 2] Drawing showing the internal configuration of the I/O bus controller of the computer system of the 1st operation gestalt.
[Drawing 3] The timing chart of each signal when operating the computing system of the 1st operation gestalt with one half of usual clock frequencies.
[Drawing 4] Drawing showing the internal configuration of the I/O bus controller of the 2nd operation gestalt.
[Drawing 5] Drawing showing the internal configuration of the I/O bus controller of the 3rd operation gestalt.
[Drawing 6] The timing chart of each signal when operating the conventional computer system with the usual clock frequency.
[Drawing 7] The timing chart of each signal when operating the conventional computing system with one half of usual clock frequencies.
[Description of Notations]
100 [-- A clock controller, 20 / -- DRAM, 21 / -- A processor, 25 / -- KBCont. (extended device) 26 / -- Clock feed zone.] -- A device controller, 1 -- A bus controller, 8 -- An I/O-bus interface controller (I/O bus controller), 11

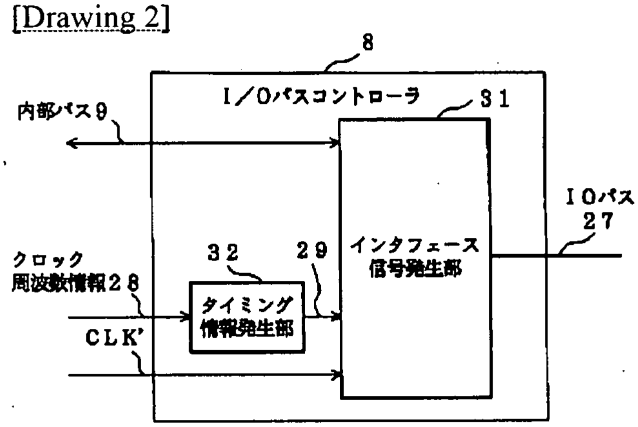
[Translation done.]

DRAWINGS

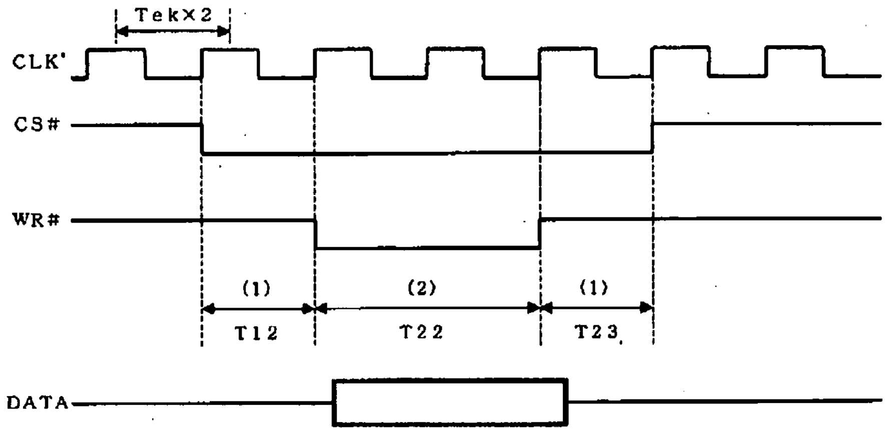
[Drawing 1]



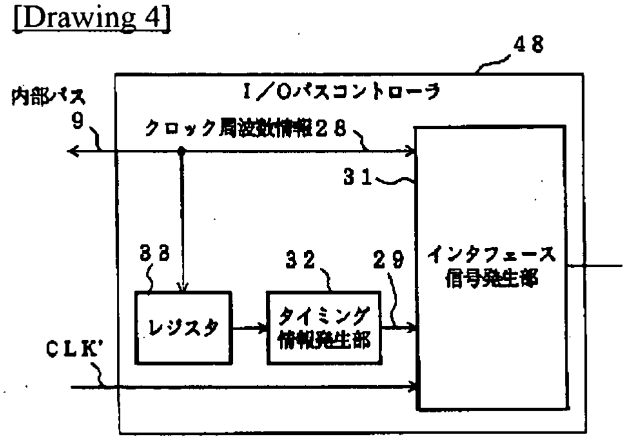
[Drawing 2]



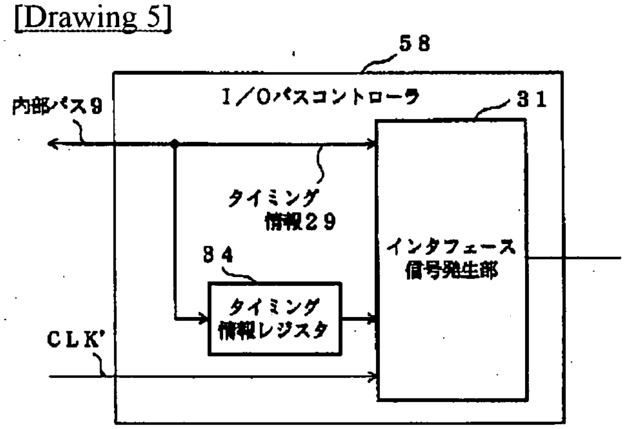
[Drawing 3]



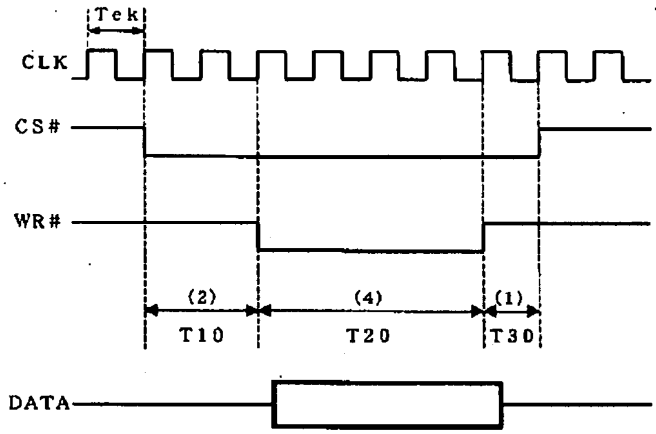
[Drawing 4]



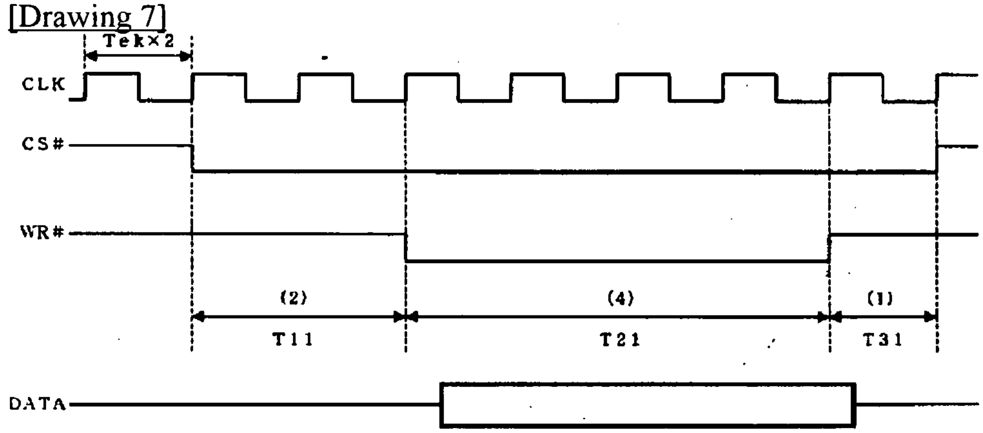
[Drawing 5]



[Drawing 6]



[Drawing 7]



[Translation done.]